D. H. Chung
J. A. Palmieri

# Design of ACP Resistor-Coupled Switching Circuits

**Abstract: Directly coupled logic circuits utilizing silicon transistors have been developed in the Advanced Circuit Program. Silicon transistors possess sufficient field gradient in the collector-base "diode" to permit high-speed operation under a forward-biased condition. Current-switching techniques provide the well-controlled voltage levels which permit operation in this region without sacrificing high speed. Operation in this region permits circuit simplification and low power dissipation.**

**A desirable state-of-the-art device is defined. Design techniques which result in a compatible set of logic circuits and power amplifiers are described. Germanium tunnel diodes are used in power driving and transmission line driving circuits.**

**In order to measure the delay times, a model with 424 circuits was subsequently built. ACP circuits (the name adopted for this circuit family) were found to perform two levels of logic in 3.2 nsec.**

## Introduction

This paper deals with the design of a set of Advanced Circuit Program (ACP) high-speed logic circuits. This family of circuits has evolved mainly from two previous developments, the current switch[1] and the cascode circuit.[2]

The underlying design philosophy of the Advanced Circuit Program lies in the technique of *current steering*, by which well-defined currents are switched with small controlling voltages. Although the current switch is logically complete as a digital circuit, it is incapable of executing (in one stage) the IMPLICATION function (which gives priority to one of the input signals). The cascode complements the current switch in performing this function. The operation of these circuits utilizes the fact that silicon epitaxial transistors may be forward-biased by 0.6 v at the collector-base junction without causing excess base charge. These circuits may thus be directly coupled, providing simple circuitry, high speed, high packaging density, and low power dissipation.

In order to test the circuits in a realistic environment a model[3] was built which contained about 1800 transistors (of the silicon planar diffused type) in 424 circuits. Measurements on this model showed that the circuits described in the present paper had average delays of 1.6 nsec per logic function.

Many high-speed logic circuits have appeared in the literature recently.[4-7] Most of these circuits claim delays of 1 nsec per logic decision but have severely restrictive fan power and logic flexibility. Experience with the system problems of high-speed, high-performance machines indicates the advantage of the logical flexibility which enables ACP circuits to compete effectively with other approaches having a lower propagation delay.

The design techniques used will be described together with certain peripheral circuits necessary for any such technology to be successful.

## Description of the circuits

The basic current-switching circuit and its graphical analysis are shown in Fig. 1. Two features are immediately apparent:

(1) Well-controlled currents are switched with small signal excursions.
(2) The devices are operated with the collectors forward-

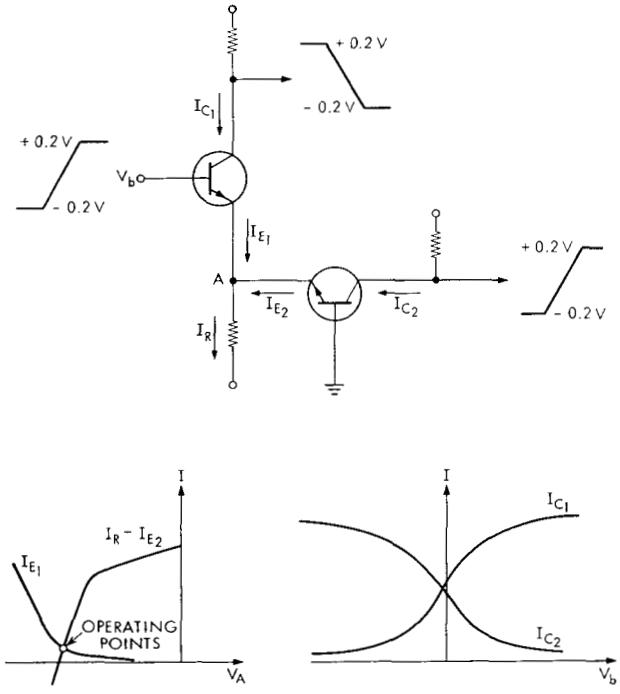
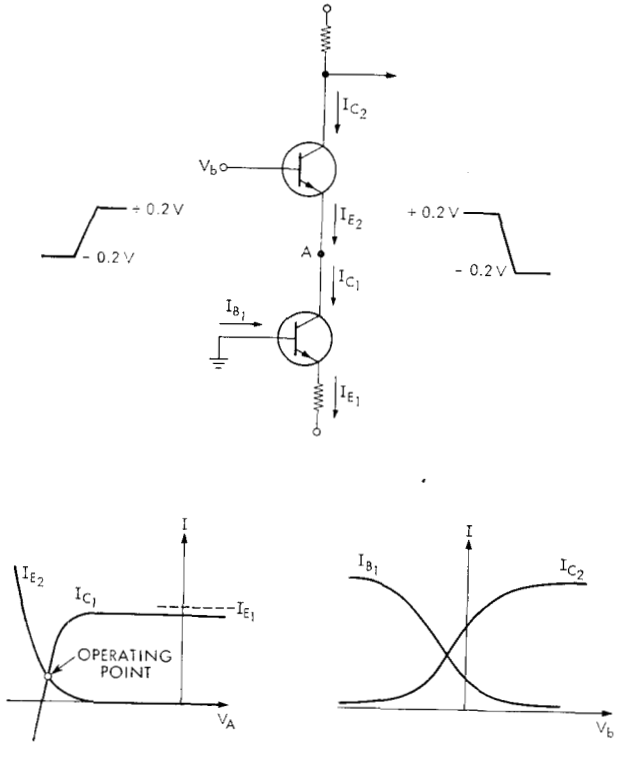



*Figure 1* **Load line analysis of basic current switch.**

*Figure 2* **Load line analysis of the cascode circuit.**



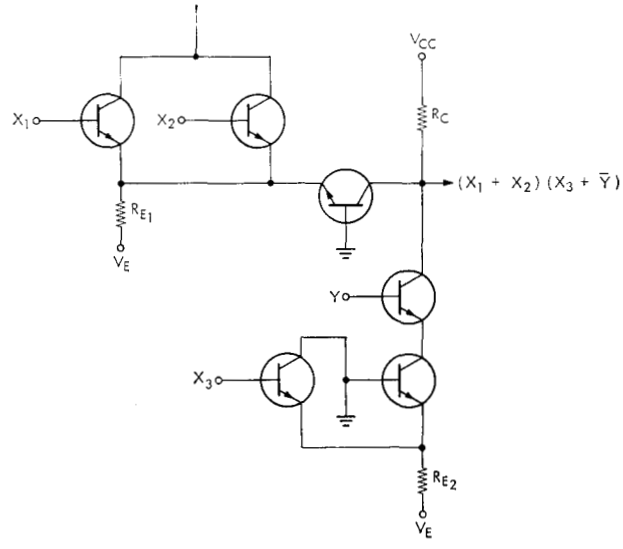




*Figure 3* **Example of WIRED-AND and IMPLICATION functions.**

biased. Such operation is possible with silicon devices since the built-in field is fairly large. Measurements have shown the excess base charge to be very small so that the high-speed performance suffers very little.

The cascode circuit is shown in Fig. 2 with its load line analysis. It can be seen that the cascode circuit operates in a manner very similar to the current switch. Paralleling transistors may extend the logic power of the cascode circuit (resulting in the IMPLICATION circuit) as shown in Fig. 3.

By connecting several collectors (of which only one is on at any one time) to a common collector resistor, a second level of logic may be performed. This is also shown in Fig. 3.

System experience has shown that the WIRED-AND and the IMPLICATION circuit greatly expand the logic power of this circuit family.

### Design objective of ACP resistor-coupled logic circuits

As we have pointed out, the logical capabilities of the basic ACP circuits can be extended by paralleling transistors. One might assume that the process of paralleling transistors can be extended indefinitely. Practical considerations, however, limit the number of permissible configurations. Implicit in Fig. 3 is the fact that only two different supplies, $V_E$ and $V_{CC}$, and three different values of resistors, $R_{E_1}$, $R_{E_2}$ and $R_C$, are used for all ACP logic circuits. It is worth while to note that the coupling resistor, $R_C$, is the same for all circuits. This feature permits the outputs of any circuit to be WIRED-AND together with any other. The value of $R_C$ is chosen to be 50 ohms. The initial goal for fan-in and fan-out of ACP is 3-and-3, i.e., at any

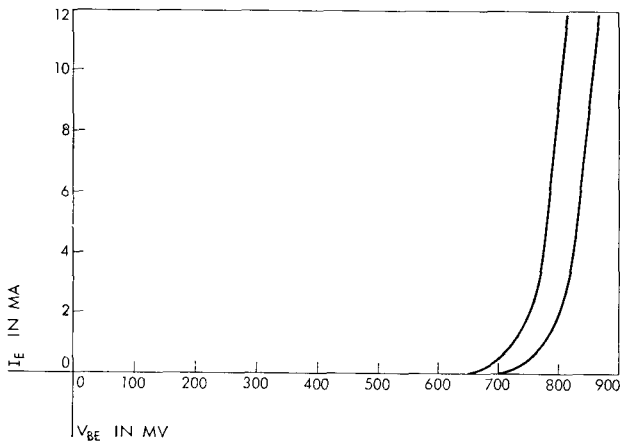



*Figure 4* $V_{BE}$ **vs** $I_E$ **limit curves.** *For* $V_{CB} = 0$, $T = 25°C$.

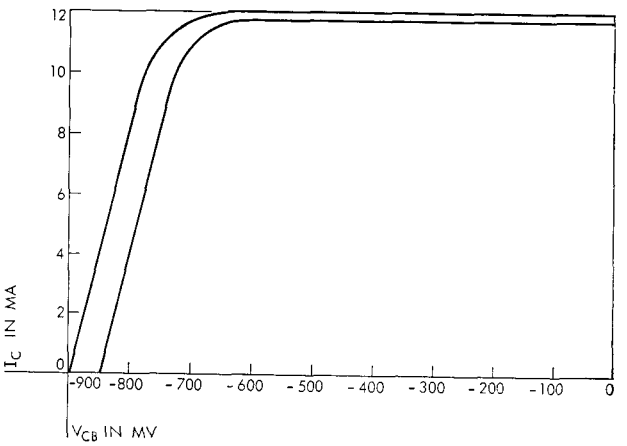



*Figure 5* $V_{CB}$ **vs** $I_C$ **limit curves.** *For* $I_E = 12$ *ma*, $T = 25°C$.

output node, three collectors can be WIRED-AND together while driving three bases from the same node. Having found a set of parameters ($R_{E_1}$, $R_{E_2}$, et cetera) satisfying this wiring requirement, we can then derive other permissible wiring configurations by extrapolating the results of the basic design.

• *Tolerances and constraints for logic circuits*

The ACP circuits are assemblies of but six elemental components: two power supplies, $V_{CC}$ and $V_E$; three resistors, $R_{E_1}$, $R_{E_2}$, and $R_C$; and the silicon epitaxial transistor. The allowable tolerances for these devices are shown in Table 1.

*Table 1* **Permissible tolerances for elemental components in ACP circuits.**

| | | |
|---|---|---|
| For $V_{CC}$: | Power supply variations: | ±1% |
| | Power distribution drop: | −2 mv |
| | Power supply noise: | ±4 mv |
| For $V_E$: | Power supply variations: | ±1% |
| | Power distribution drop: | −2 mv |
| | Power supply noise: | ±20 mv |
| For all resistors: | | ±1% |
| For the silicon epitaxial transistor: | | $\beta_{\min} = 30$ |
| | | $V_{be}$: See Fig. 4 |
| | | $V_{cb}$: See Fig. 5 |
| Temperature range: | | 25 to 50°C |

$\partial V_{cb}/\partial_T = \partial V_{BE}/\partial_T = 1.5$ to 1.7 mv /°C

In the design of high-speed circuits with delays approaching 1 nsec, important considerations include the following:

(1) The signal swing should be kept as small as practicable in order to minimize the delay due to stray capacitance. But a small voltage swing requires close level control to maintain its logical identity.

(2) Nonsaturating transistor operation is required to preserve the high-frequency characteristics of the semiconductor. This constraint places an upper limit on the maximum voltage swing.

(3) Transmission of signal over a long distance is incompatible with nanosecond circuits. Thus, the logical net must be composed of small parts with a high packaging density, and the component circuits must contain a minimum number of devices.

(4) Lower power dissipation is in keeping with the above requirements of small swing, minimal delay, and miniaturization.

(5) The role of packaging for both system and circuit in nanosecond technology is important in minimizing unnecessary delays due to power distribution and other auxiliary effects.

(6) A set of useful switching circuits must necessarily possess a high degree of logical flexibility in addition to its high speed. From an over-all system viewpoint, power in performing logic functions is of great practical importance.

In addition to these prerequisites for the design of high-speed circuits, circuit reliability is, of course, a perennial concern to the circuit designer. The solutions to reliability problems are approached with various design philosophies such as the end-of-life and worst-case design. The design of ACP circuits utilizes conservative statistics to give a quantitative estimate of the built-in safety factor. From the experience accrued, one may conclude that the statistical method, circumspectly applied, not only reveals much of the hidden potentiality of the circuits but also serves as a useful compass in design.

• *Design of logic circuits*

The dc gain curve shown in Fig. 6 is a useful design aid. An in-phase switching circuit with a range of conditions (parameter tolerances, fan-in and fan-out) exhibits the two limiting gain curves shown in the Figure.

From this plot, the noise tolerance of the circuit may be readily determined. The term *noise tolerance* refers to the maximum amplitude of spurious noise, the effect of which will diminish rather than accumulate when propagating through a chain of similar circuits.

Since no reactive elements are used in ACP circuits, the dc plots include the worst cases. The methods of obtaining the dc gain curve for the entire ACP logic circuit family are discussed below. It is clear, first of all, that the output voltage of any ACP circuit is directly proportional to its output current since the coupling resistor $R_C$ is equal to 50 ohms for all ACP circuits. Thus,

$$V_O = V_{CC} - R_C I,$$

where

$V_O$ = output voltage of an ACP circuit

$I$ = output current of an ACP circuit

$R_C$ = 50 Ω, the coupling resistor

$V_{CC}$ = collector supply voltage whose magnitude is to be determined.

Our problem, therefore, is one of finding the output current, $I$, at different values of input voltages. This calculation involves not only the nonlinear characteristics of the transistors but also device tolerances and temperature variations. The most expedient method is a graphical solution, which has been programmed on a digital computer. The resultant plot assumes the form shown in Fig. 7 for the in-phase output of the current switch.

Similar curves are plotted for the out-of-phase output of the current switch and the cascode circuit. A load line formed by the collector resistor (50 Ω) and $V_{CC}$ is then placed on these characteristics. Algorithmic procedures have been developed to vary the parameters such that the three following criteria are satisfied:

(1) Fan-power objectives are met.

(2) Satisfactory noise tolerance is obtained.

(3) The maximum signal swing does not cause saturation.

A set of parameters which meet these criteria have the following values:

$R_{E_1} = 357\Omega$ $\quad V_{CC} = 255$ mv

$R_{E_2} = 340\Omega$ $\quad V_E = -4.5$ v

$R_C = 50\Omega$

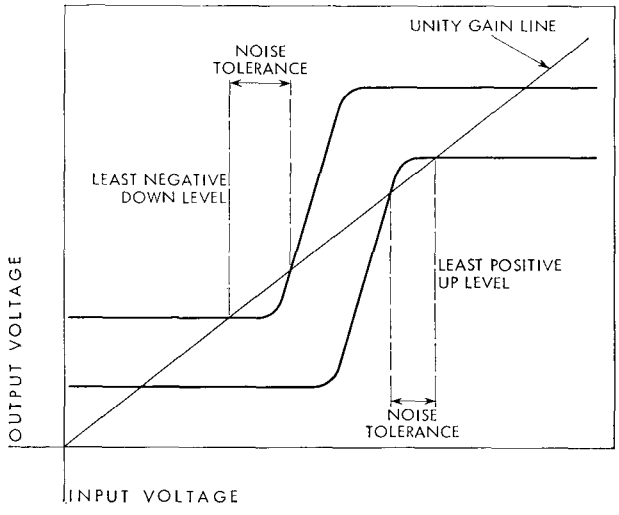
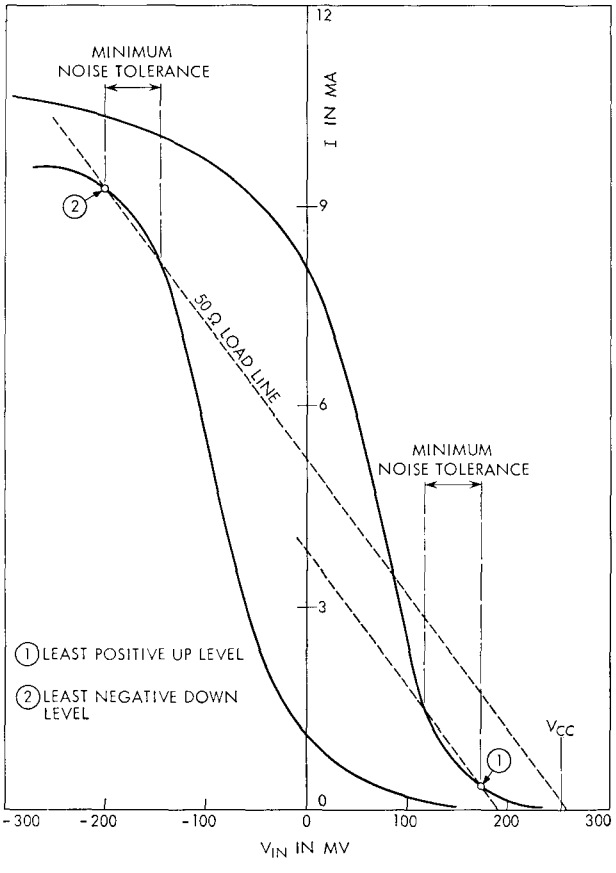
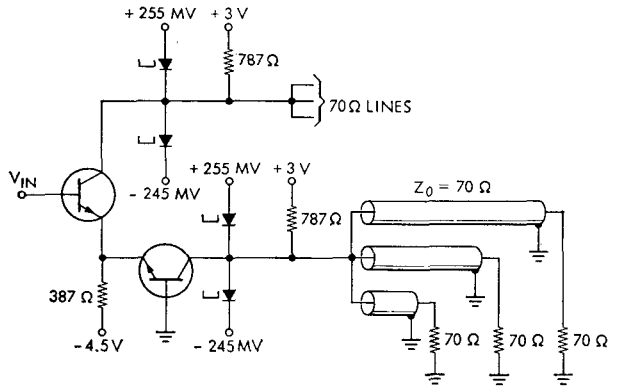


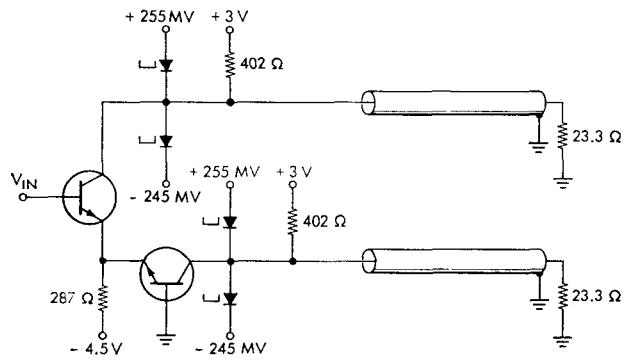

*Figure 6* **Direct current gain curve.**

*Figure 7* **Limiting transfer function curves for in-phase output of current switch in most-critical circuit configurations.** *Maximum* ON *current, out of phase, 50°C; minimum* ON *current, in phase, 25°C; maximum leakage, 50°C; $R_{E1} = 357$ ohms.*





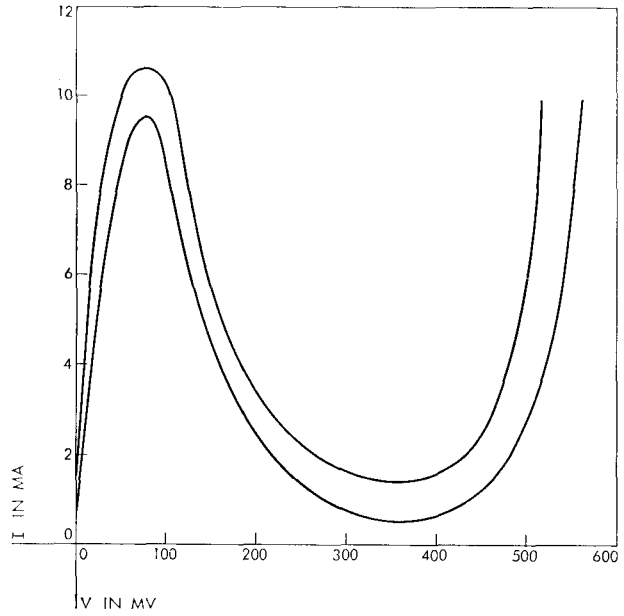

(a)




(b)

*Figure 8* **Power amplifiers in the ACP circuit family.** *(a) Line driver. (b) Power driver.*

*Figure 9* **Limit curves of the ACP tunnel diode.** *25°C < T < 50°C; $C_j$ @ $V_v$ : 10 pf; $L_s$ : 0.6 nh.*




Following the procedures outlined in the Appendix, we made normal fits to the base current and collector off-currents with the following resulting parameters:

$I_b$: mean value, $m = 0.175$ ma
standard deviation, $\sigma = 0.065$ ma

$I_L$: mean value, $m = 0.15$ ma
standard deviation, $\sigma = 0.035$ ma.

From these figures a fan-power table may be generated such that the failure rate does not exceed $10^{-3}$.

*Table 2* **Permissible wiring configuration at any output node.**

| *No. of Collectors* | *No. of Bases* | *Failure Probability* |
|---|---|---|
| 6 | 1 | $1 \times 10^{-4}$ |
| 5 | 2 | $2.9 \times 10^{-4}$ |
| 4 | 2 | $1 \times 10^{-4}$ |
| 3 | 3 | $1 \times 10^{-4}$ |
| 2 | 4 | $1 \times 10^{-4}$ |
| 1 | 5 | $6 \times 10^{-4}$ |

We wish to emphasize that the above failure rates are those of specifically wired nodes under the worst temperature, input level, power supply and resistor variations. It is important to note that any individual ACP circuit has a failure rate far less than the figures quoted above. Furthermore, failure probability for connections less severe than any of the entries in Table 2 is less than the tabulated value. For example, if three collectors and two bases are connected to a node, the failure probability is less than 1 case out of 10,000.

With the design values, the minimum noise tolerance for both negative and positive noise pulse is 55 mv.

## ACP power amplifiers

There are two types of power amplifiers in the ACP family, namely, the line driver, Fig. 8a, and the power driver, Fig. 8b.

The line driver is capable of driving three 70-ohm transmission lines at either of its outputs. A maximum of two bases can be driven from any line. The power driver can drive 18 bases from a 70-ohm line at either collector. Germanium tunnel diodes are used to provide power amplification and signal level clamping. The output voltage levels of the drivers are compatible with the logic circuits. Figure 9 shows the characteristics of the tunnel diode. Tunnel diodes are used in pairs to eliminate any variance at the output due to a different transition at the input. Both circuits have a statistical failure rate of 1 in 1000 under the worst temperature, input level, and supply variations.

The line driver can be made to serve as a memory element by proper connection with a logic circuit. Figure 10 shows the line driver in the current switch configuration is WIRED-AND to a cascode, forming a trigger.

The function of this trigger is to sustain or memorize a "data" signal for a period of time corresponding to the interval between two consecutive "clock" pulses. The maximum system "clock" rate at which this circuit can function reliably is 100 Mc.

The power amplifier circuits require two additional supplies (+3.0 v, −245 mv) and six different values of resistors which are not included in the logic circuits. The tolerances for these additional elements are:

For +3.0 v supply: same as $V_E$ (see Table 1)
For −245 mv supply: same as $V_{CC}$ (see Table 1)
All resistors: ±1%

The detailed design of the tunnel diode coupling network is similar to that described by Murphy and Turnbull[8] and therefore is not discussed here.

## Test model

In order to test the concepts of the ACP circuits, a 20,000-transistor Arithmetic and Logical Unit was designed. An 1800-transistor model was abstracted and built which included sufficient worst-case and control paths for a realistic test of the timing relationships. Details are given in Ref. 3.

An average of 2.2 nsec per level of logic was observed in the worst-case path of the model. Of this 2.2 nsec, 1.6 nsec is the logic function delay and the remaining 0.6 nsec may be attributed to wire propagation and power driver delays.

## Conclusions

The extreme versatility of ACP circuits can be seen from the wide variety of member circuits[3] and the broad latitude for wiring the output node (see Table 2). The objective design includes a minimum noise tolerance of 55 mv at either logical level. Experiments on crosstalk between worst-case transmission line configurations have shown that a tolerance of 55 mv is more than sufficient to insure proper logical operation. The inherent nature of the current-steering mechanism and the unique feature of WIRED-AND gives rise to an over-all delay of 2.2 nsec per logic decision. The ACP circuits are thus capable of operating at a system rate of 100 Mc. The quoted failure rate of 1 case per 1000 is a conservative estimate, valid only at the most unfavorable temperature, input swing, and power supply values. In the ACP circuits the power dissipation per logic circuit is under 50 mw. This low value of dissipation allows high density of packaging, thus minimizing the propagation delay.

A measure of the high-speed operation that can be achieved with ACP circuits can be seen from the addition time of 0.2 μsec (for 64-bit floating point operands) which was achieved in the model.

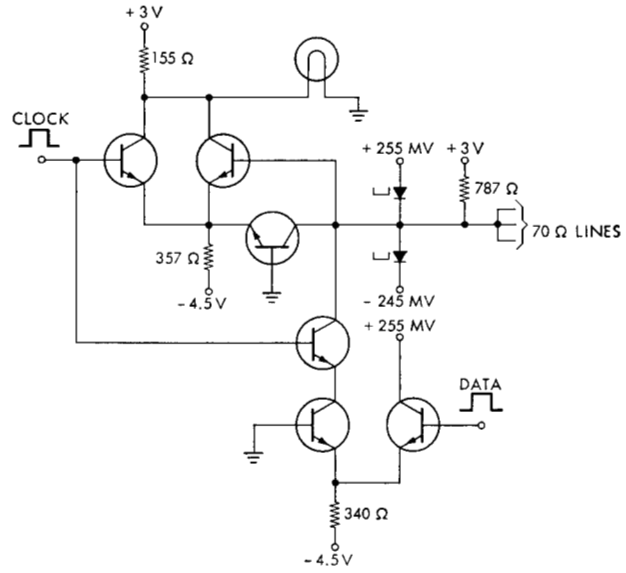



*Figure 10* **ACP trigger circuit.**

## Appendix: Statistical analysis of leakage currents

• *The problem and the approach*

There are two types of leakage currents in ACP circuits, namely, the collector leakage current, $I_L$, and the base leakage current, $I_b$. The total leakage current at a given node is a summation of $I_L$ and $I_b$ at that node. A statistical study of total leakage thus requires not only the knowledge of the frequency distributions of $I_L$ and $I_b$, but also a method of combining them. This analysis involves three major steps:

(1) To formulate the probability density function, PDF, of the parameters of the circuit components by measurements.

(2) To derive the PDF's of the emitter currents by graphical methods.

(3) To determine the PDF of the total leakage currents by applying suitable probabilistic variable transformations.

• *Formulation of* PDF*'s of the circuit components*

A sample of 5000 transistors for ACP circuits was tested for the forward current gain, $\beta$, base-emitter characteristic, and the collector-base characteristic at constant emitter currents. The density function of $\beta$ is shown in Fig. 11. The measurements of the transistor characteristics show that slightly more units fall near the center of specified spreads (see Figs. 4 and 5) than at the edges. Thus uniform distributions for transistor characteristics are assumed since these distributions give statistical worst cases.

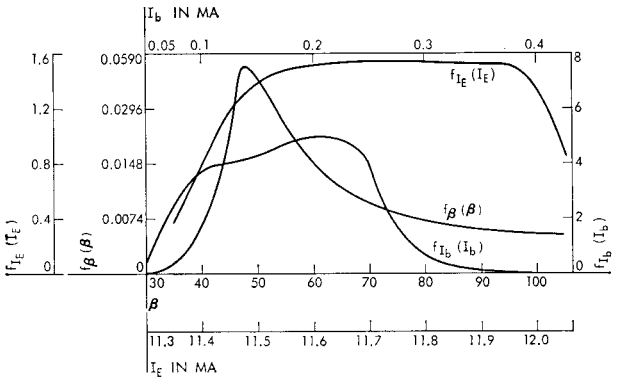



*Figure 11* **Distribution of $\beta$, $I_B$, and $I_b$.**

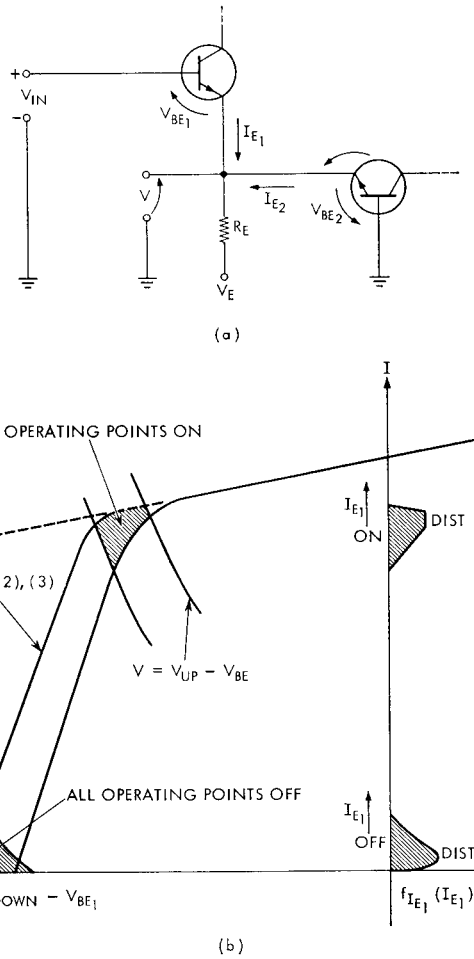



*Figure 12* **Method for determining $I_E$ distributions.** *(a) Kirchhoff's equations. (b) The graphical method.*

• *Graphical determination of* PDF*'s of emitter currents*

To clarify the graphical method of determining the PDF's of the emitter current, let us consider the specific case in Fig. 12a.

The relevant Kirchhoff's equations are:

$$V = I_R R_E + V_E \tag{1}$$

$$V = -V_{BE_2} \tag{2}$$

$$I_{E_1} = I_R - I_{E_2} \tag{3}$$

$$V = V_{in} - V_{BE_1} \tag{4}$$

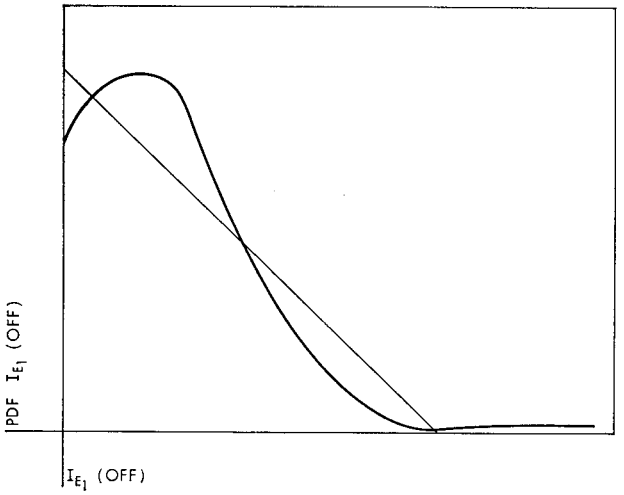
The independent variables of the above equations are $R_E$, $V_E$, $V_{BE_1}$, $V_{BE_2}$ and $V_{in}$. Because of the nonlinear nature of the transistor, the solution can best be obtained by graphical techniques. Since each of the independent variables contains a range of values, the solutions are necessarily multivalued, as is indicated in Fig. 12b.

Since the transistor characteristics are assumed to be uniformly distributed, any value of current in the cross-hatched region has a given probability of occurrence. The frequency distribution is obtained by measuring the width of the cross-hatched area at a given current, and by plotting this width versus the current as shown in Fig. 13. In order to convert this frequency distribution to a probability density function the $f_{I_{E_1}}(I_{E_1})$ axis must be scaled such that

$$\int_{-\infty}^{\infty} f_{I_{E_1}}(I_{E_1})\, dI_{E_1} = 1. \tag{5}$$

Notice that $I_{E_1}$ (off) is distributed such that a triangular fit (Fig. 13) may be made for simplicity in calculation. This approximation is a conservative estimate.

*Figure 13* **Triangular fit of the probability density function of $I_{E_1}$ *(off)*.**




• *Probabilistic variable transformations*

The base current of a transistor can be calculated by the following relationship:

$$I_b = I_E/(1 + \beta). \tag{6}$$

The worst-case base current can be calculated by using the maximum $I_E$ and minimum $\beta$. Circuit designers are occasionally obliged to use the worst-case figures in the absence of statistical distributions of the independent random variables.

But, should the distributions of the independent variables be known, it will be highly desirable to have a quantitative knowledge of the safety factor inherent in the design. The problem here is thus equivalent to finding the PDF of a dependent variable, $y$, from the given PDF's of the random variables, $x_1, x_2, \cdots, x_n$. The functional relationships are:

$$y = g(x_1, x_2, \cdots, x_n) \tag{7}$$

and its unique inverse,

$$x_1 = h(y, x_2, \cdots, x_n). \tag{8}$$

Then

$$f_y(y) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\left|\frac{\partial h}{\partial y}\right| f_{x_1,x_2,\cdots,x_n}$$

$$\times[h(y, x_2, \cdots, x_n), x_2, \cdots, x_n]\, dx_2\, dx_3 \cdots dx_n, \tag{9}$$

where

$f_y(y)$ = PDF of $y$,

and $f_{x_1,x_2,\cdots,x_n}(x_1, x_2, \cdots, x_n)$ = joint density function of $x$'s.

The validity of Eq. (9) is conditioned upon:

(1) The function $y = g(x_1, x_2, \cdots, x_n)$ is monotonic for all values of each $x$ where its PDF is nonzero.
(2) The inverse function $x_1 = h(y, x_2, \cdots, x_n)$ is unique and all first order partial derivatives exist.

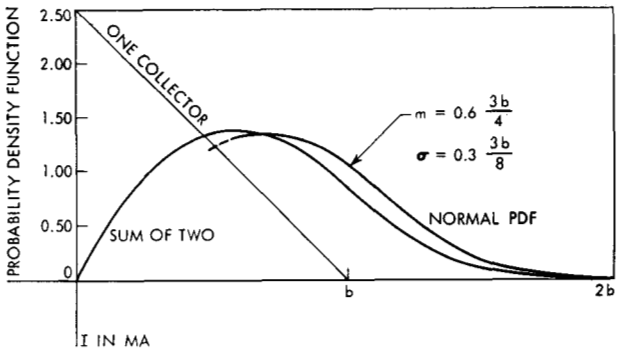
For the case where $I_b = I_E/(1 + \beta)$, and its inverse function, $\beta = (I_E - I_b)/(I_b)$, if the PDF of the emitter current and the forward current gain are given to be $f_{I_E}(I_E)$ and $f_\beta(\beta)$ respectively and if $I_b$ and $\beta$ are independent in a probability sense, then

$$f_{I_b}(I_b) = \int_{-\infty}^{\infty}\left|\frac{\partial \beta}{\partial I_b}\right| f_{I_c}(I_E) f_\beta(\beta[I_{E_1} I_b])\, dI_E. \tag{10}$$

An approximate formula derived from the above equation can be used to evaluate $f_{I_b}(I_B)$ numerically.

$$f_b(I_b) \approx \sum_{I_E} \frac{I_E}{{I_b}^2} f_\beta\left(\frac{I_E}{I_b} - 1\right) f_{I_E}(I_E)\Delta I_E. \tag{11}$$

*Figure 14* **Probability density function for sum of two (triangular distributions) independent random variables.**



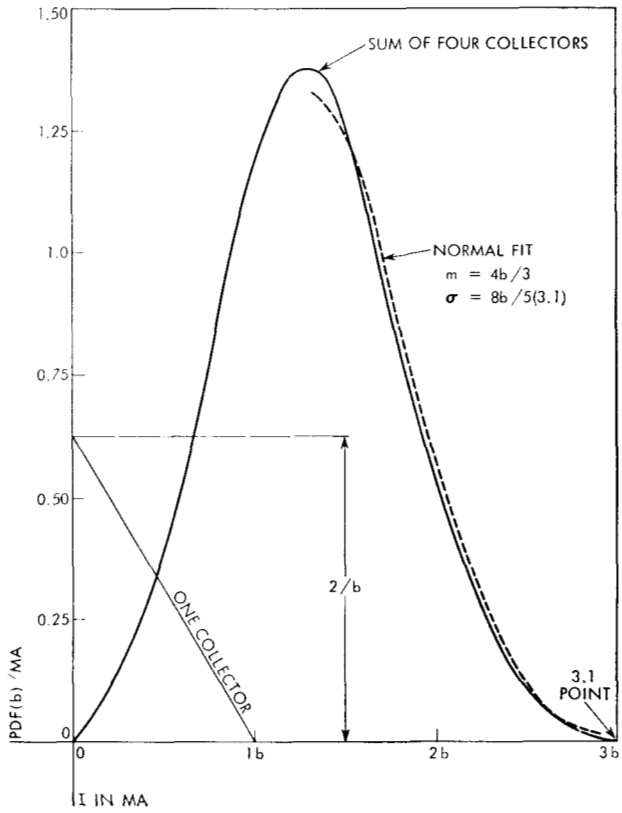




*Figure 15* **Probability density function for sum of four variables, each with triangular distribution.**

Figure 14 shows the derived density function of $I_b$ along with those of $I_E$ and $\beta$.

For a particular case where $y = x_1 + x_2 + \cdots + x_n$, and where $f_{x_1}(x_1) = f_{x_2}(x_2) = \cdots f_{x_n}(x_n) = f_x(x)$. The density function, $f_y(y)$, can be derived analytically by repeated application of the convolution integral. Through the use of complex variable and Laplace transformation, however, the convolutions can be performed by raising the Laplace transformed density function, $\mathcal{L}[f_x(x)]$, to the $n^{th}$ power. The function, $f_y(y)$, is obtained by taking the inverse Laplace of $\{\mathcal{L}[f_x(x)]\}^n$. Figures 14 and 15 show the results of this method for the density functions of the leakage current for sums of two and four collectors, respectively. The density function of a single collector leak-

age is postulated to be triangular as described previously.

The methods mentioned above are mathematical stratagems for multivariate probability transformation, and the resultant density functions are not necessarily of the form convenient for engineering manipulation. The derived density function serves, however, as a valuable basis for an approximation to a normal distribution. The selected normal distribution must represent a conservative estimate of the original density function. Thus, it is possible to characterize the density function of the base current $f_{I_b}(I_b)$, by specific values of the mean, $m$, and the standard deviation, $\sigma$ (see Figs. 14 and 15). Now if the distribution of total base currents of three bases is required, the rules governing the addition of independent normal variables can be applied, i.e.,

$$m_{\text{total base current}} = 3m$$
$$\sigma^2_{\text{total base current}} = 3\sigma^2.$$

With the knowledge of these parameters, circuits can be designed with a known failure rate.

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